

FIG. 1A

ASYNCHRONOUS SUBACTION

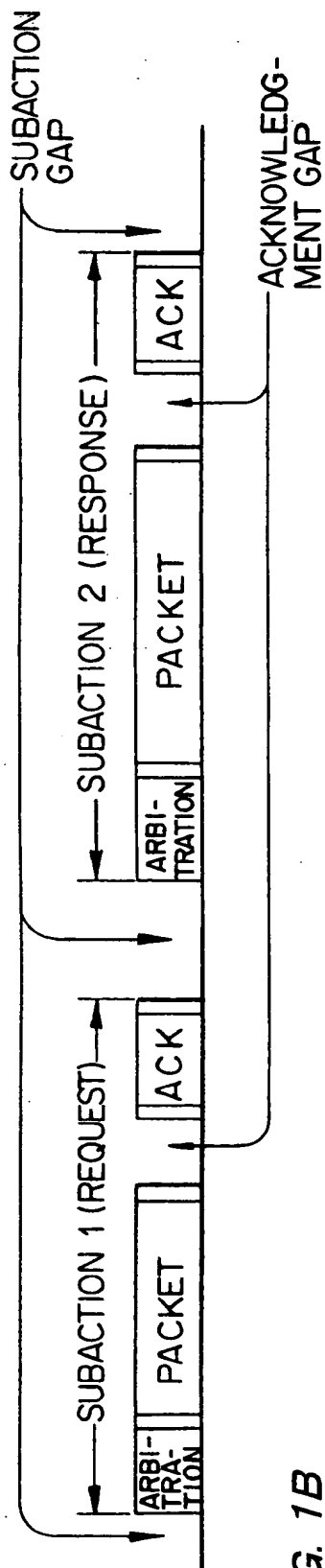


FIG. 1B

ISOSYNCHRONOUS SUBACTION

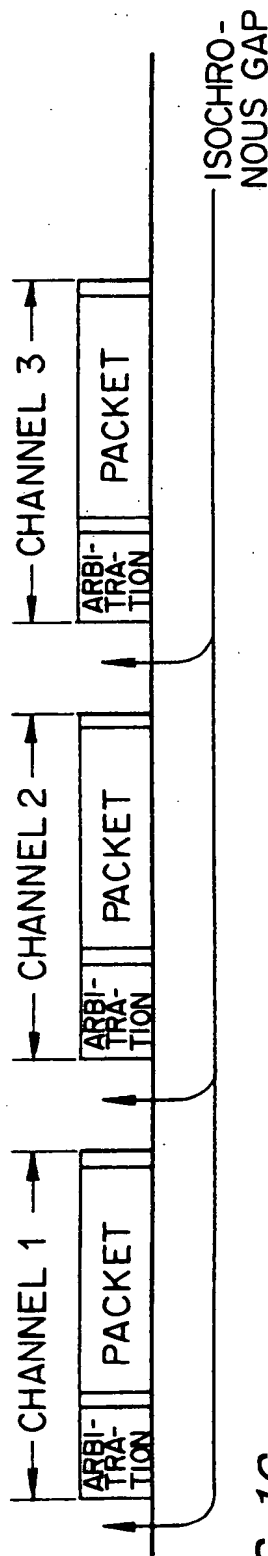


FIG. 1C

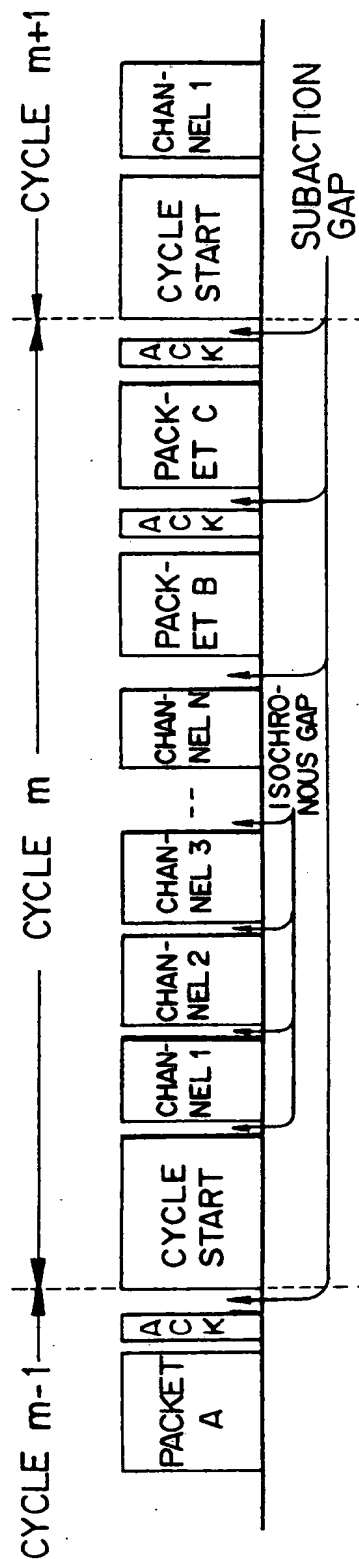


FIG. 2A

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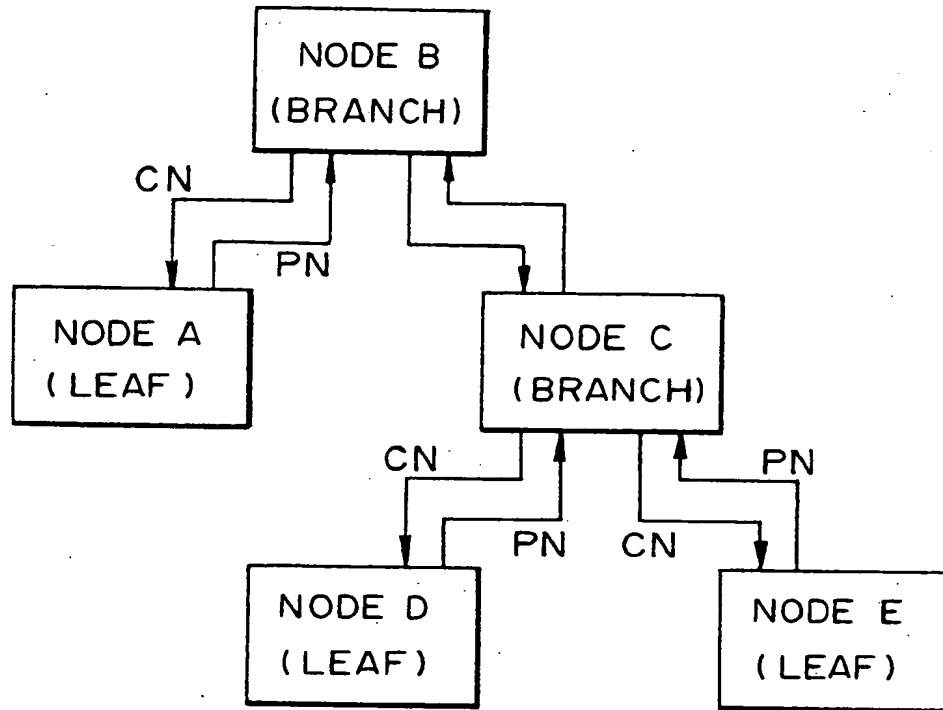


FIG. 2B

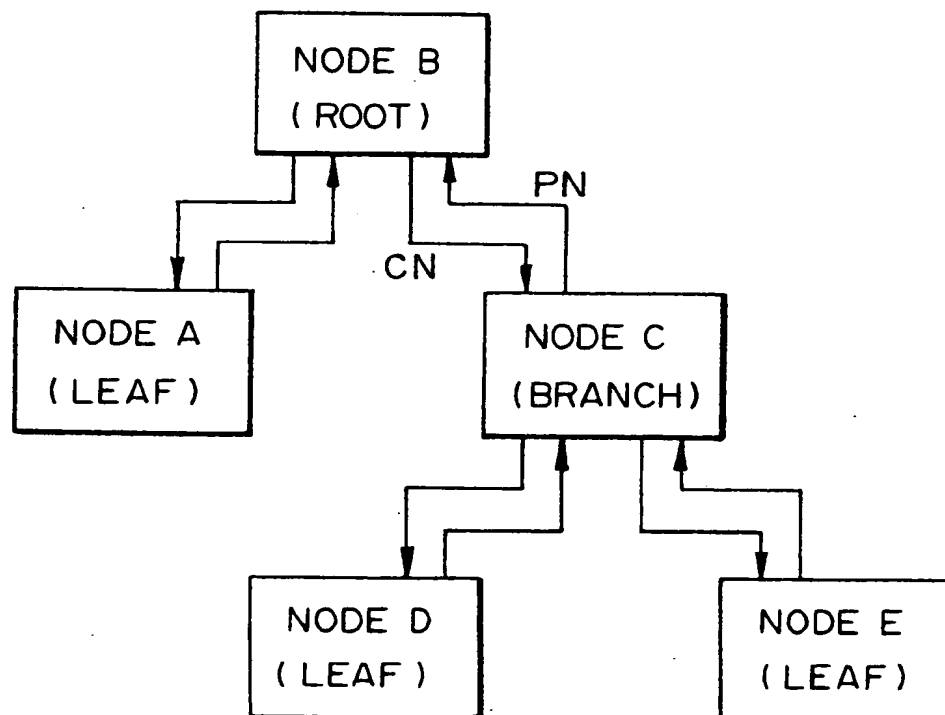
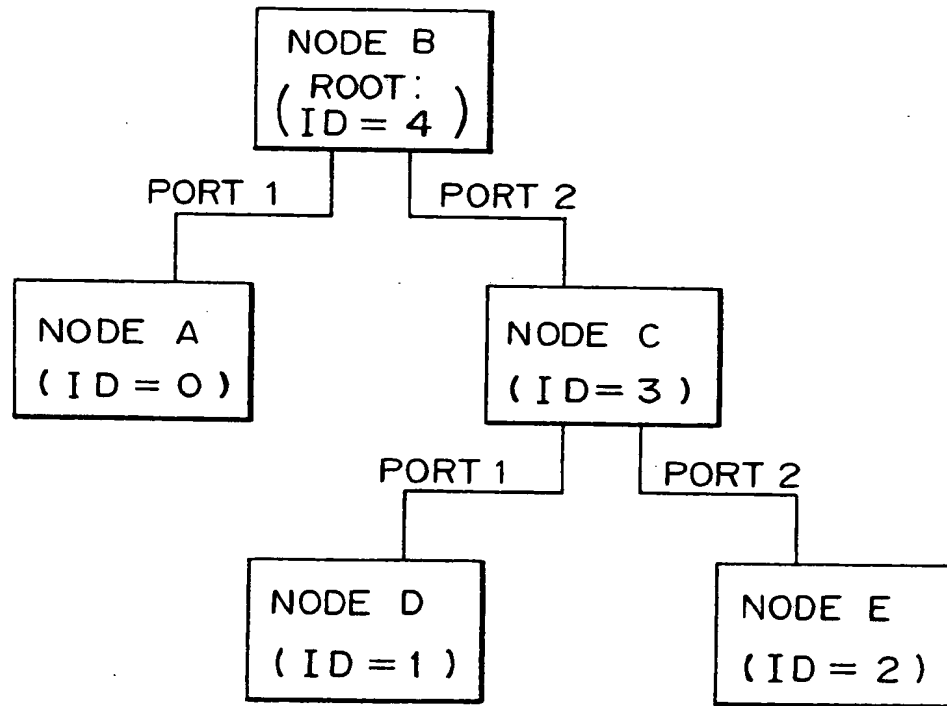


FIG. 3



**FIG. 4B**

## LINK-ON PACKET

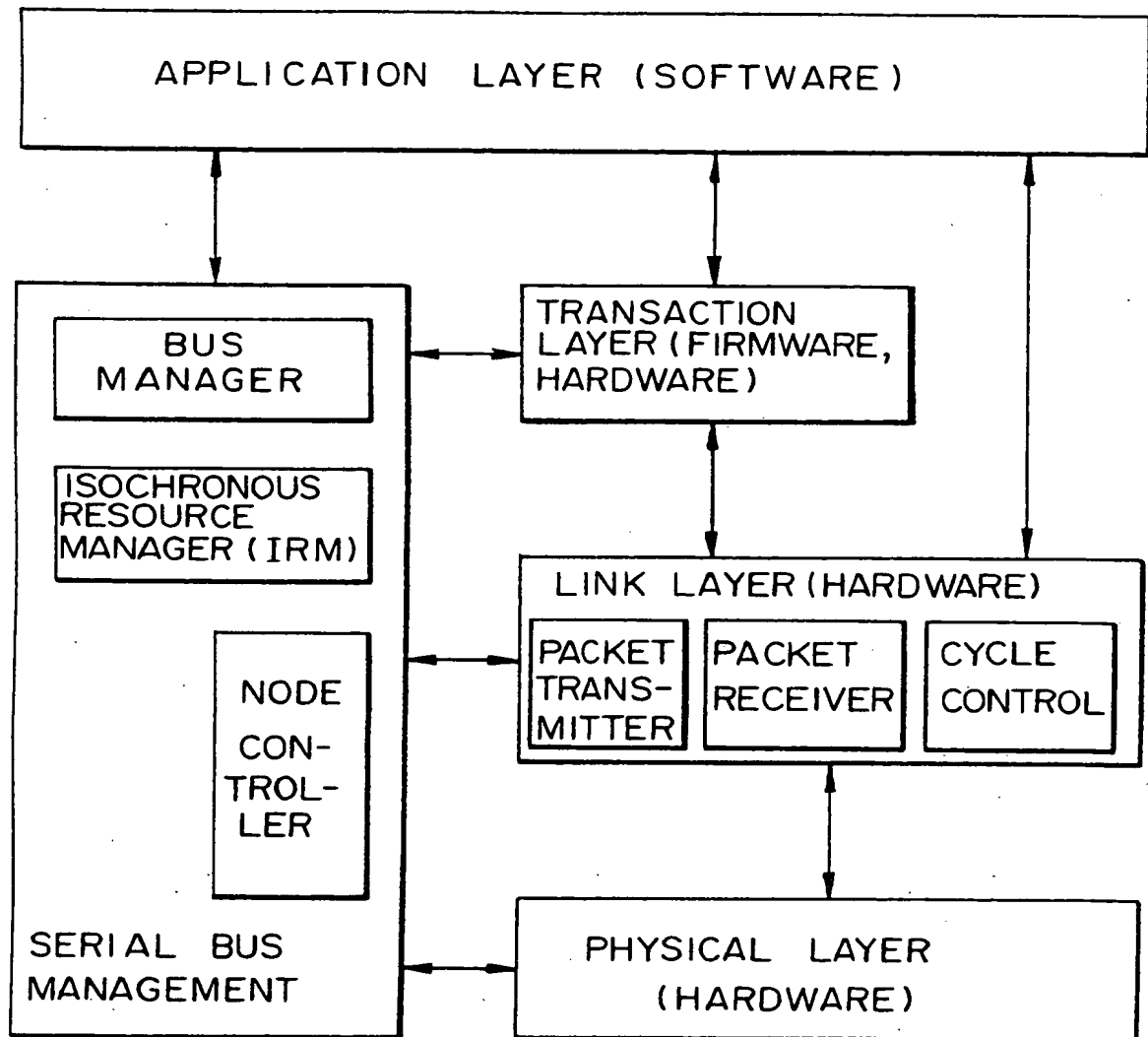
	b.31															b.0
0	10	PHY_ID	1	n	rsv	pa	pb	pc	pd	pe	pf	pg	ph	r	m	
1	INVERSION OF FIRST 32 BITS															

**FIG. 4D**

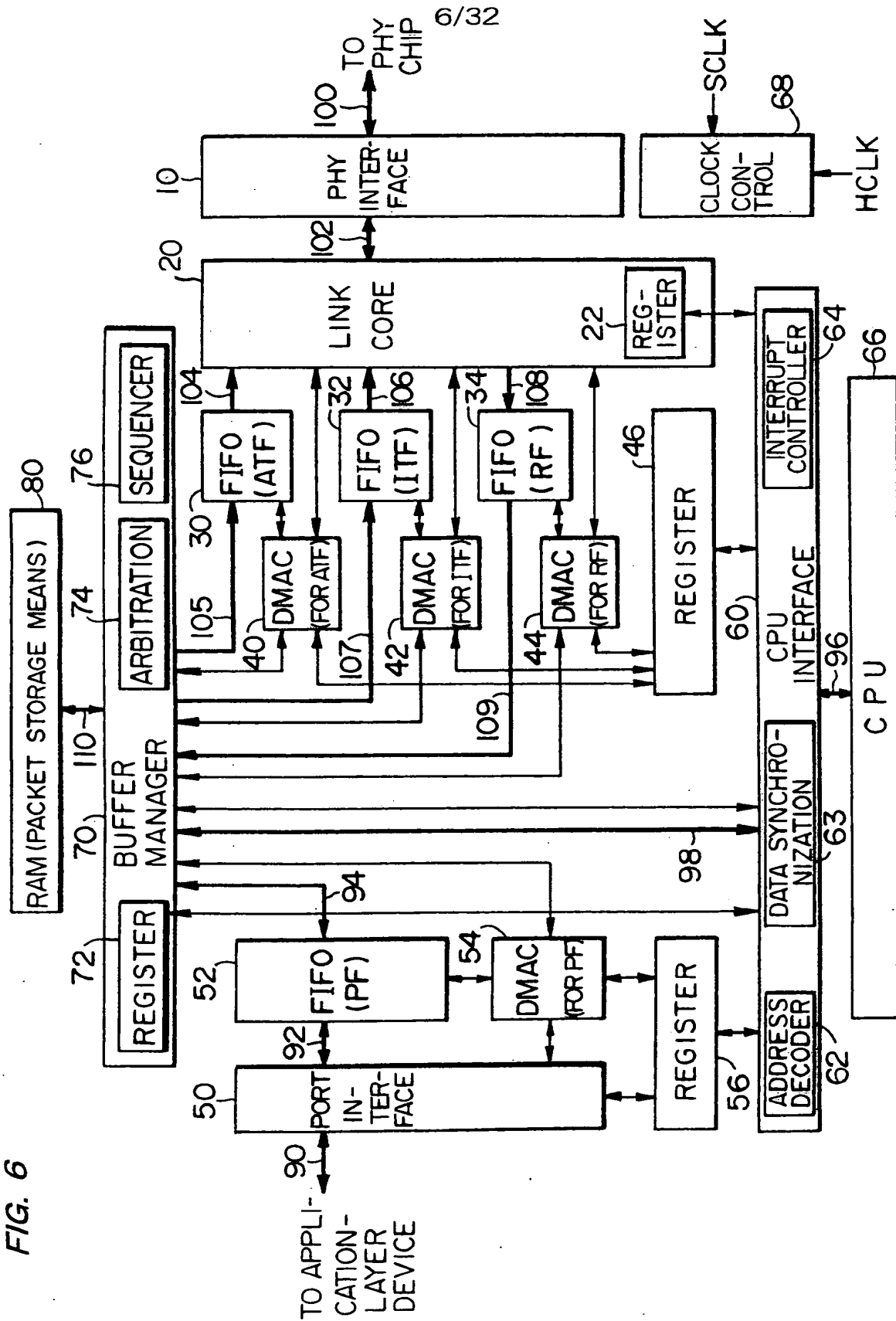
	b.31										b.0									
0	00	PHY_ID	R	T	gap_cnt	0000	0000	0000	0000											
1	INVERSION OF FIRST 32 BITS																			

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FIG. 5



**FIG. 6**



**FIG. 7**

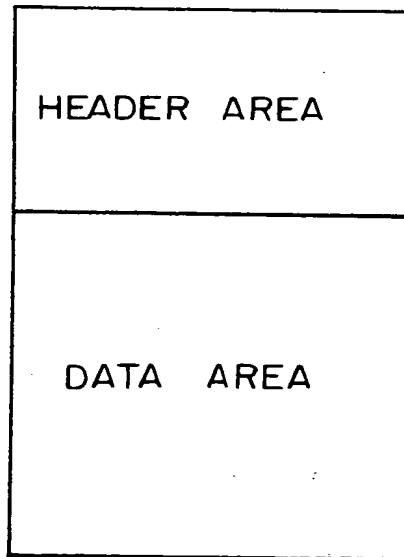
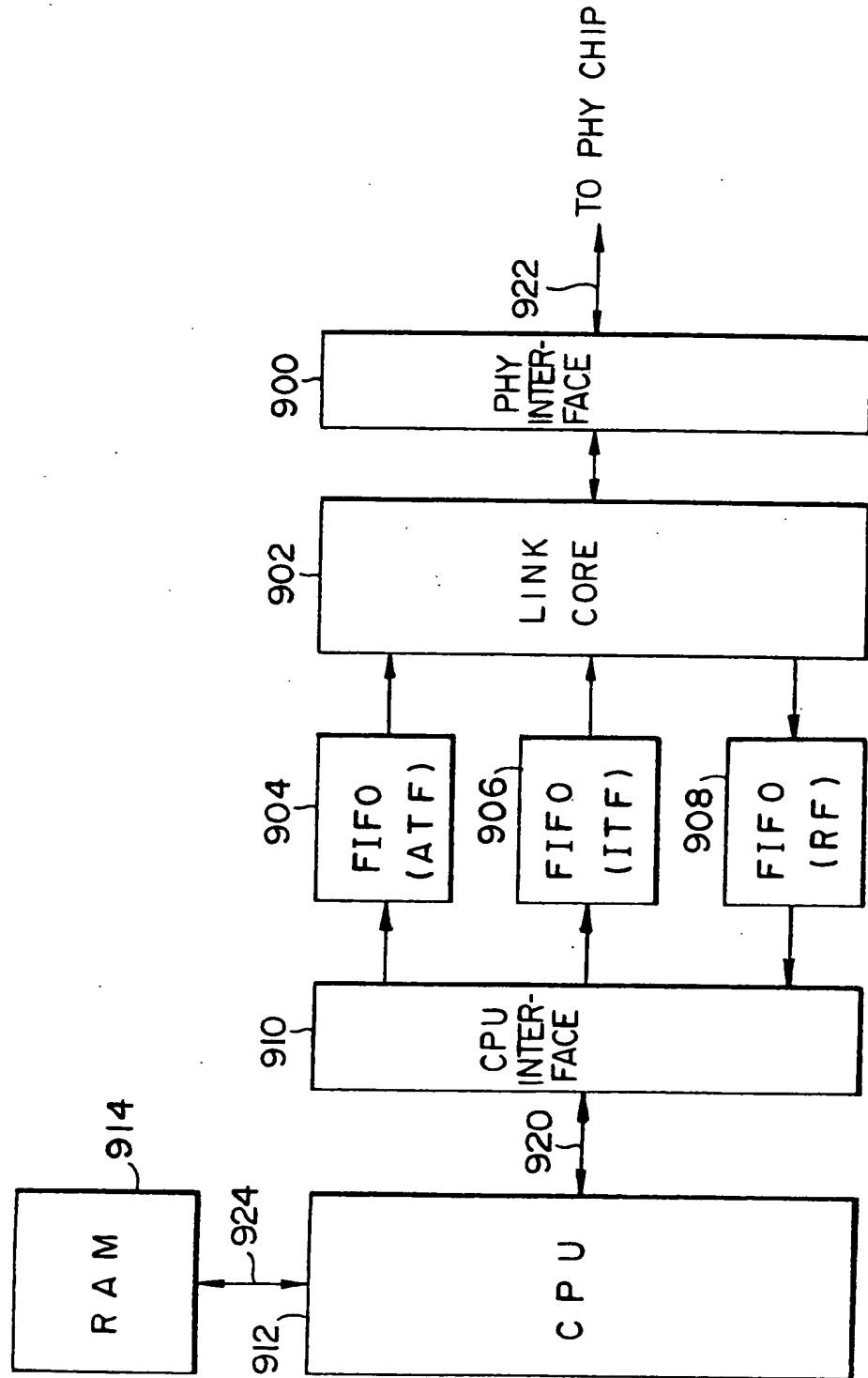


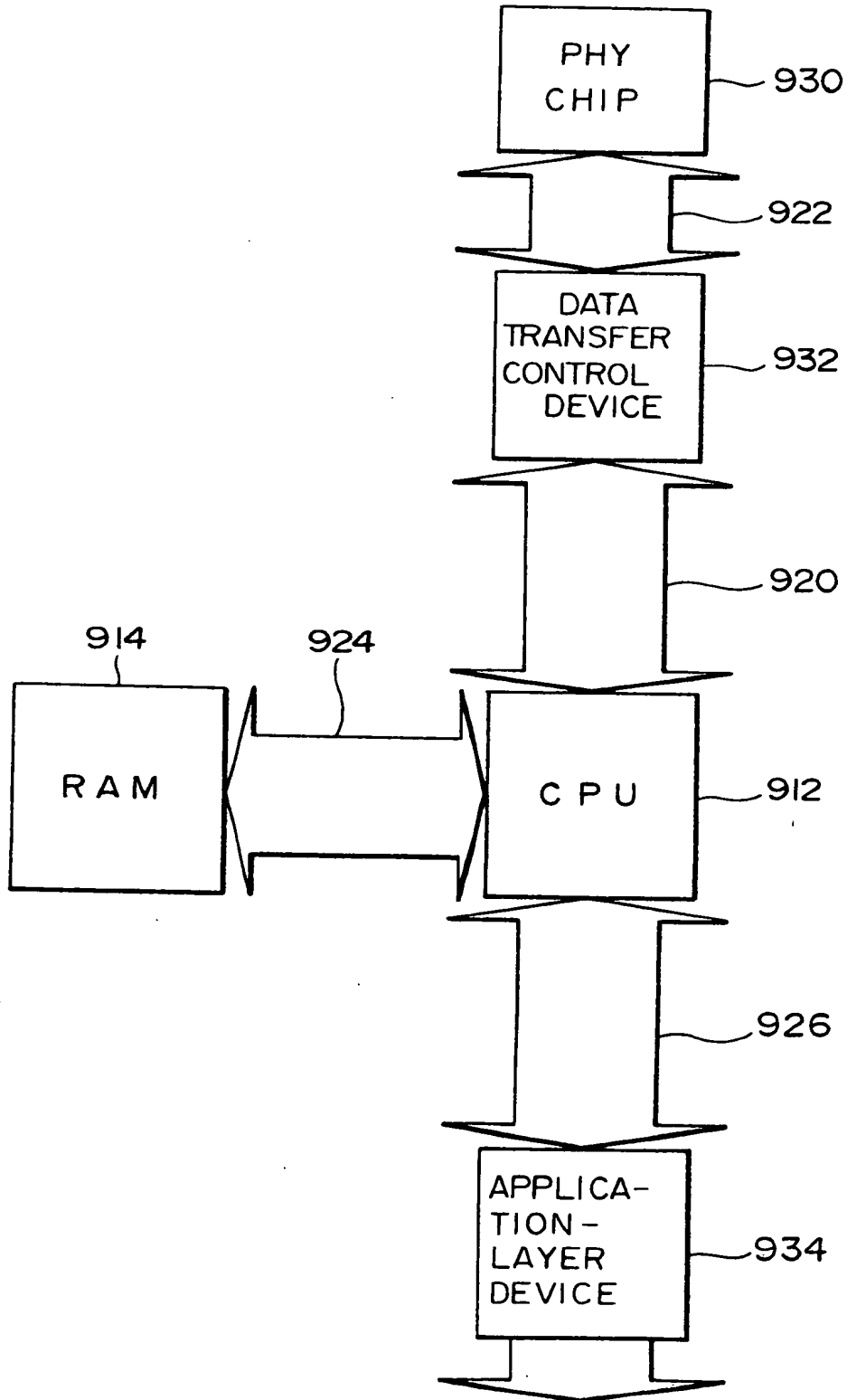
FIG. 8





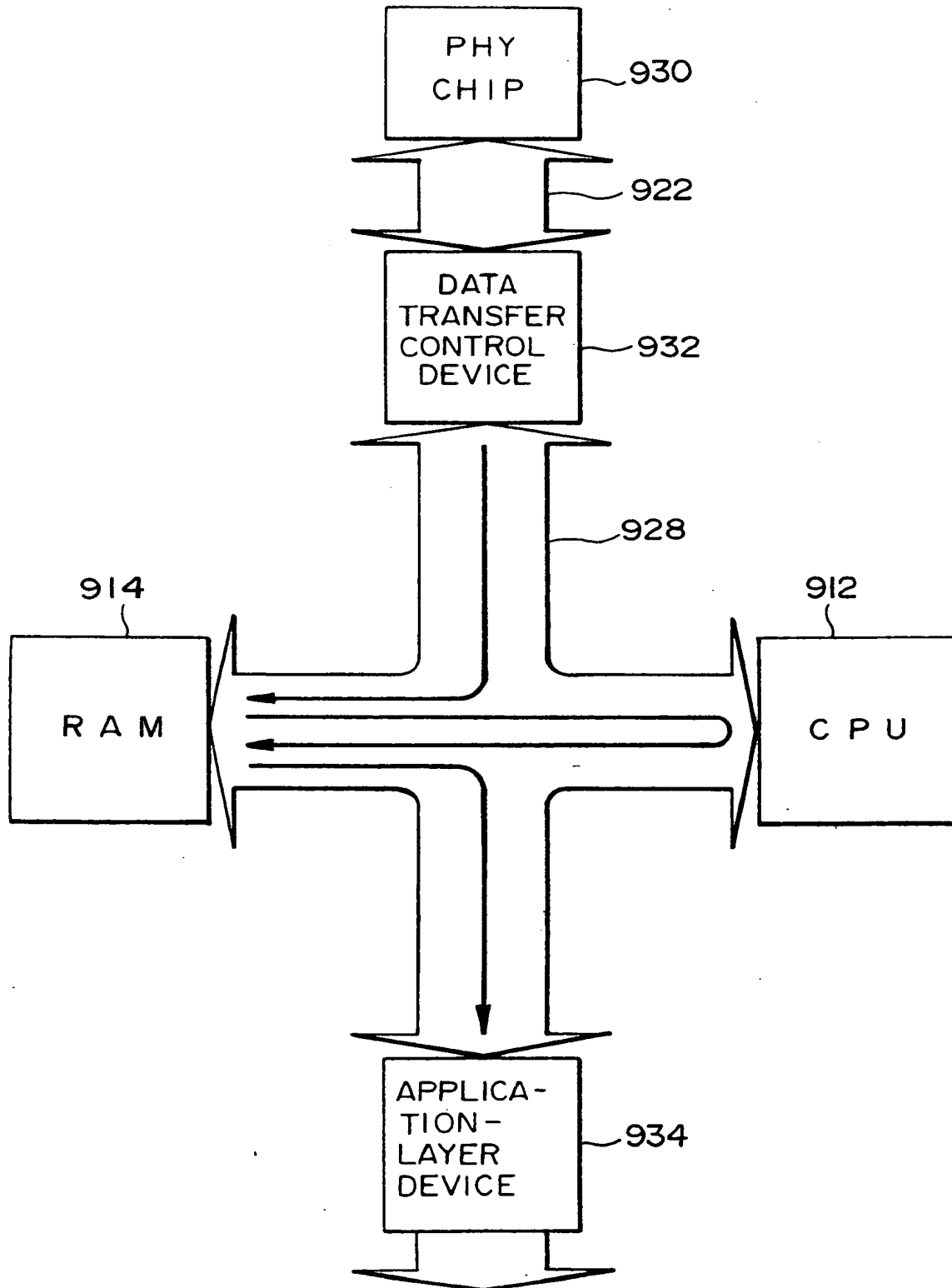
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FIG. 9



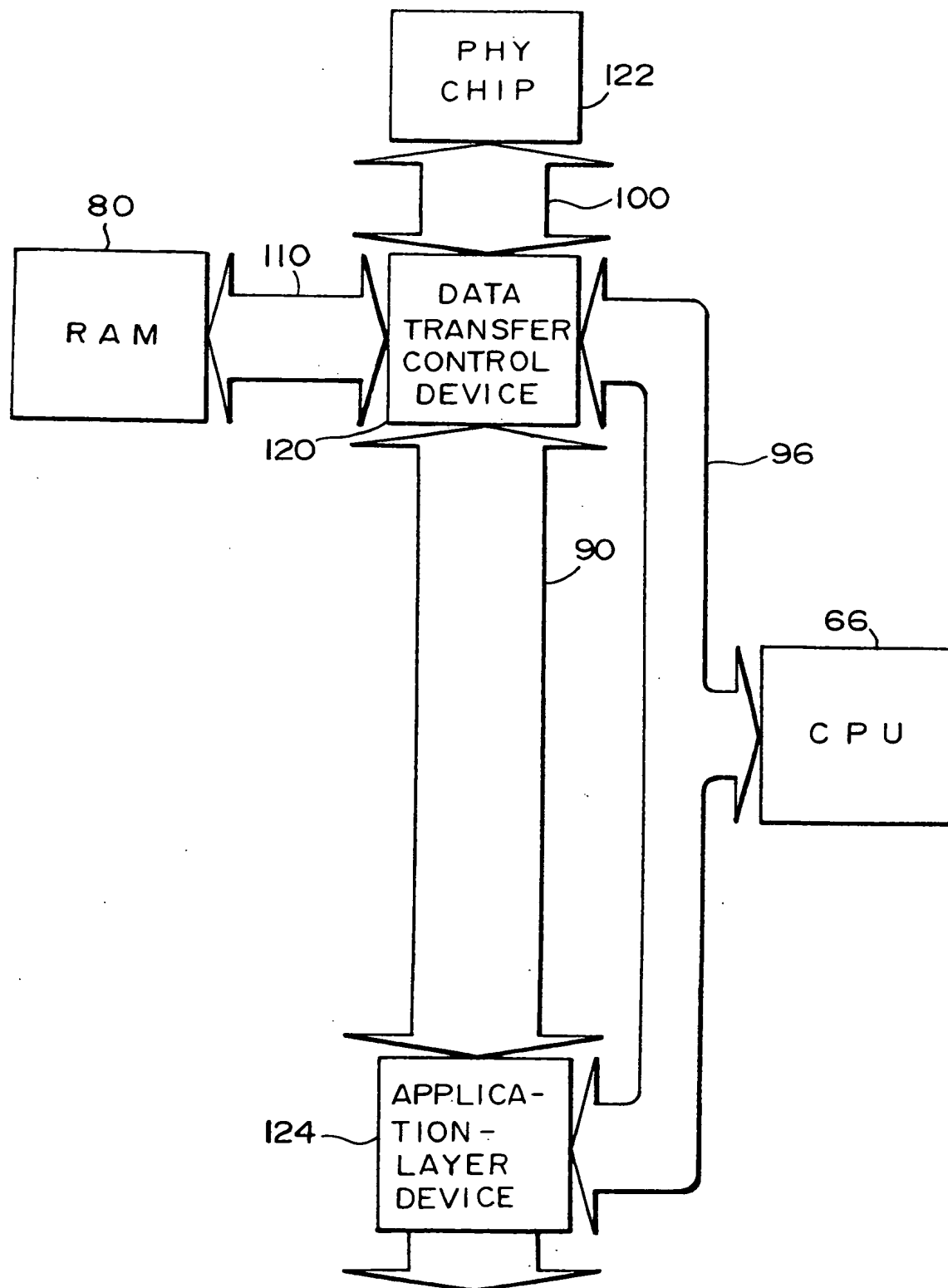
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FIG. 10



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FIG. 11



**FIG. 12**

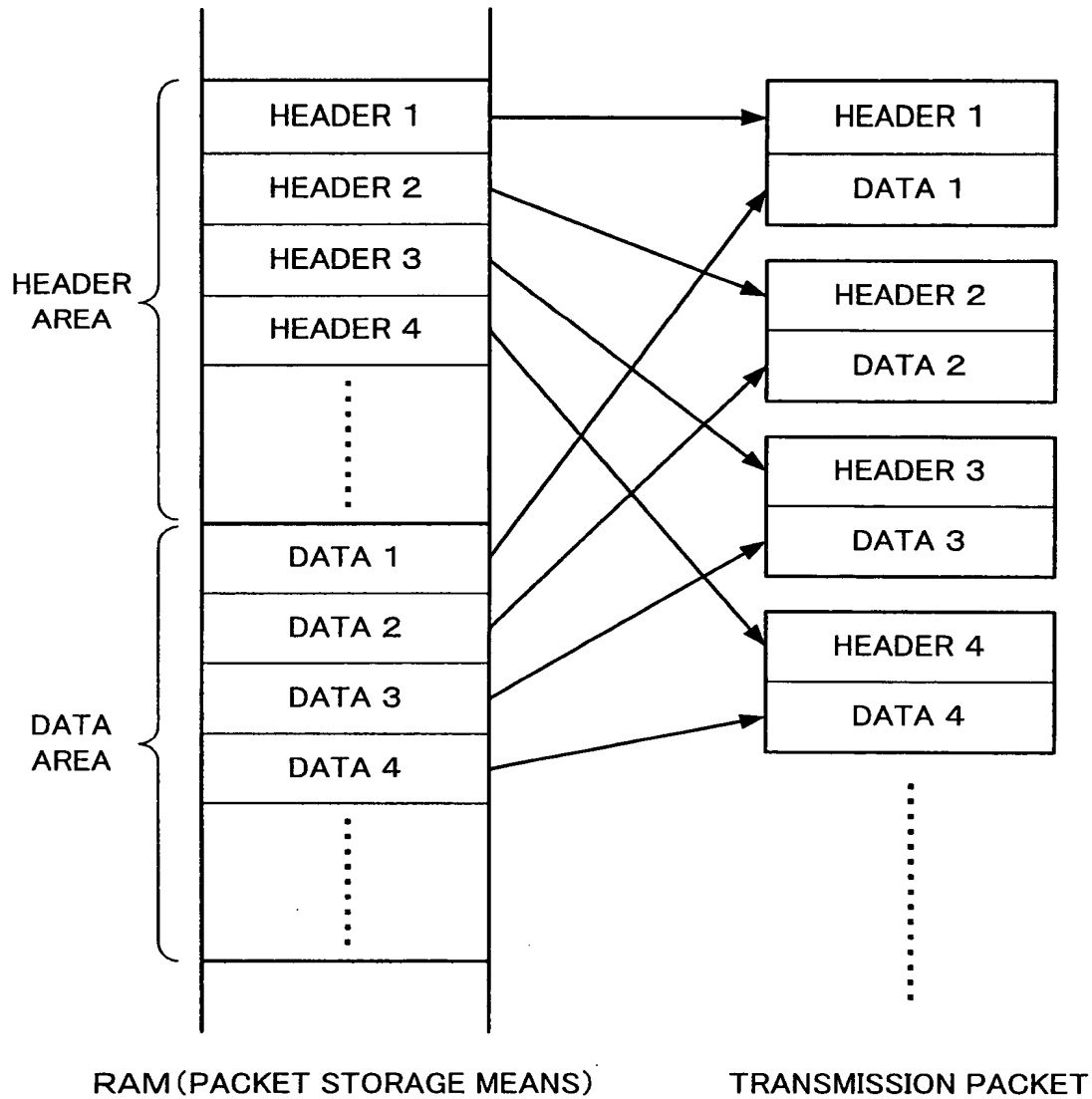
[illegible]

FIG. 13

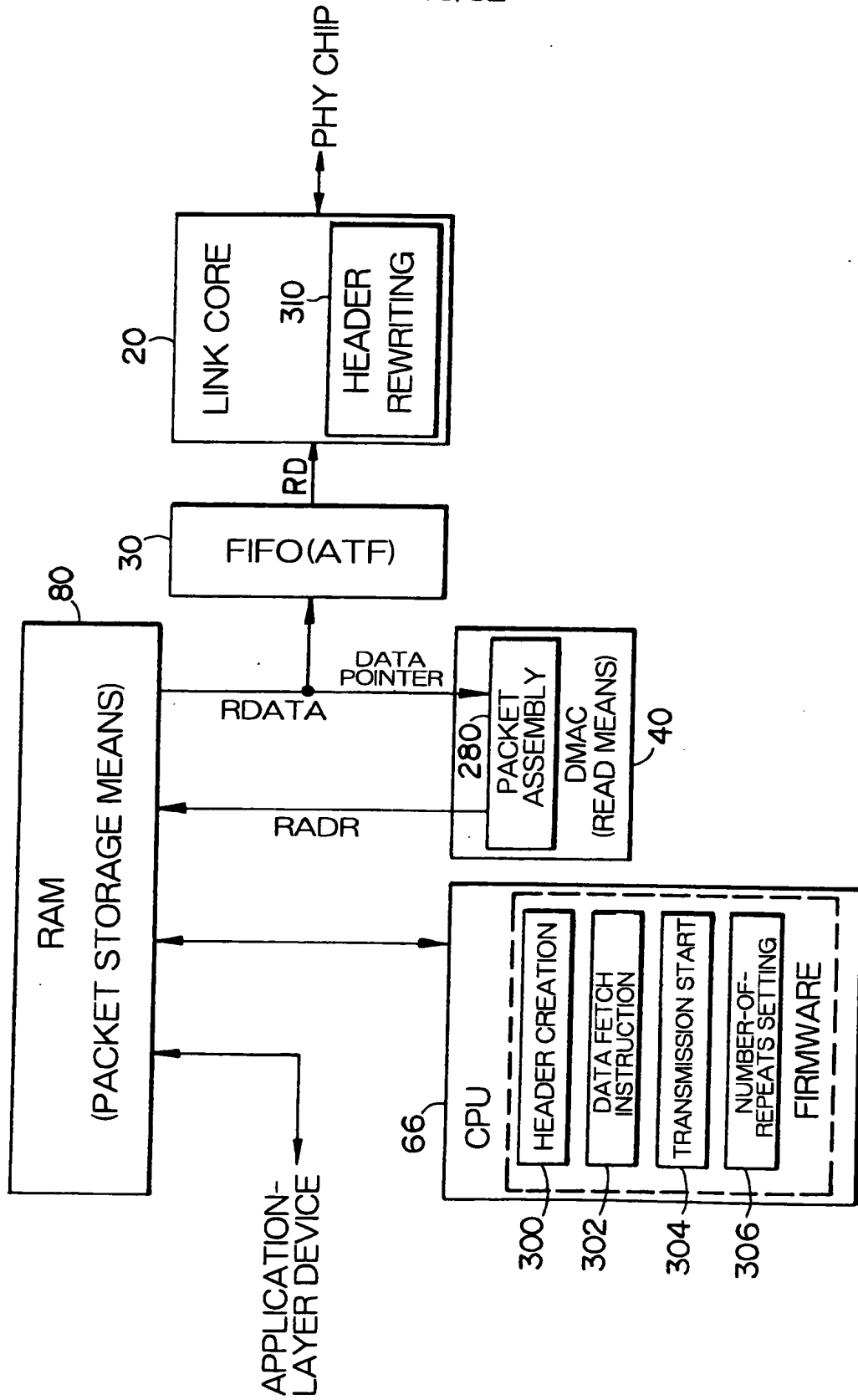
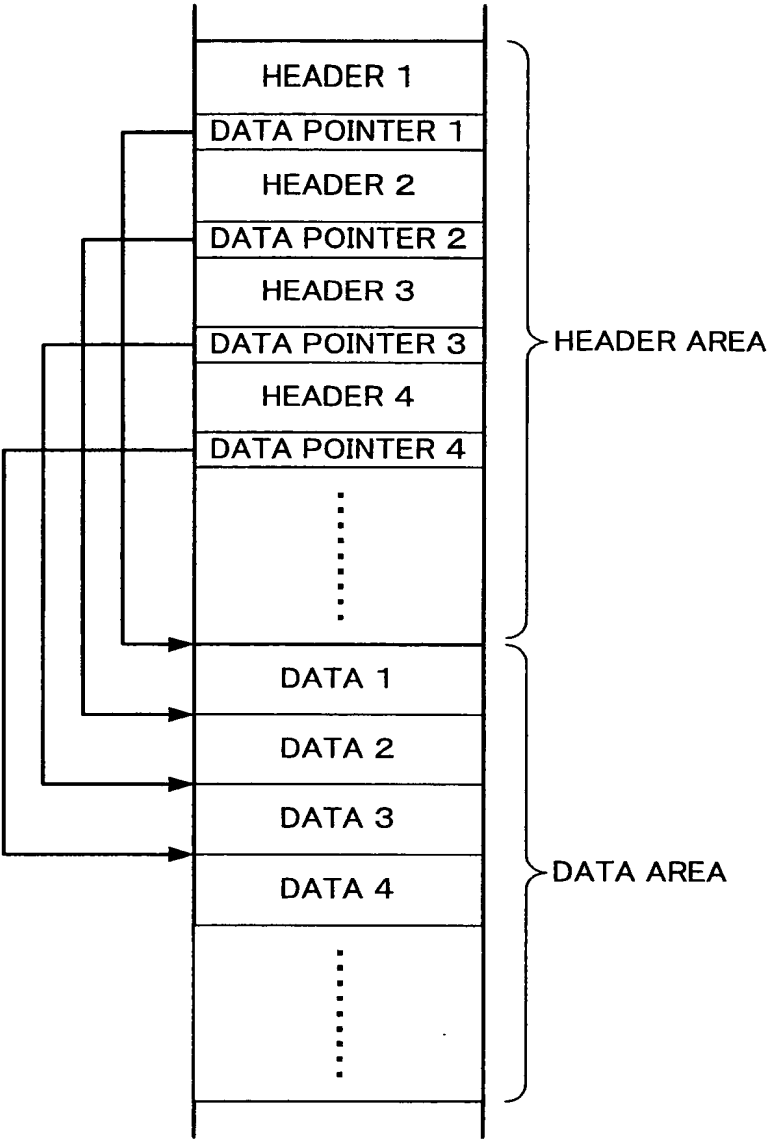


FIG. 14

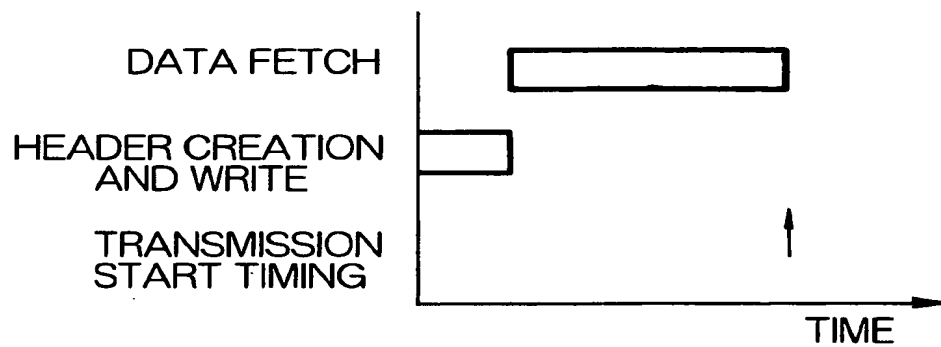


RAM(PACKET STORAGE MEANS)

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**FIG. 15A**

COMPARATIVE EXAMPLE

**FIG. 15B**

THIS EMBODIMENT

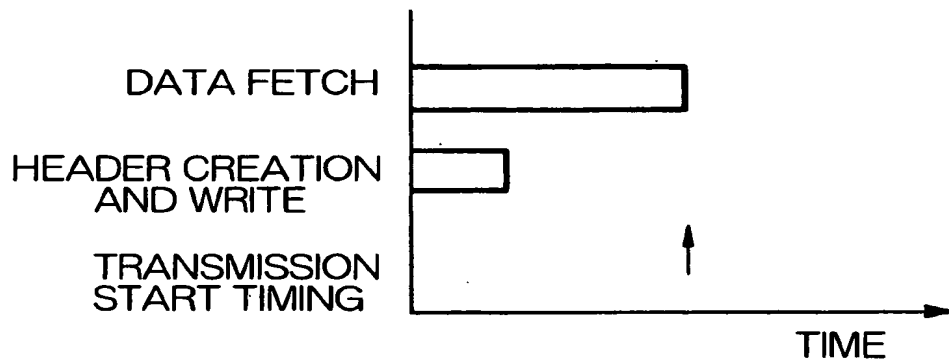


FIG. 16A

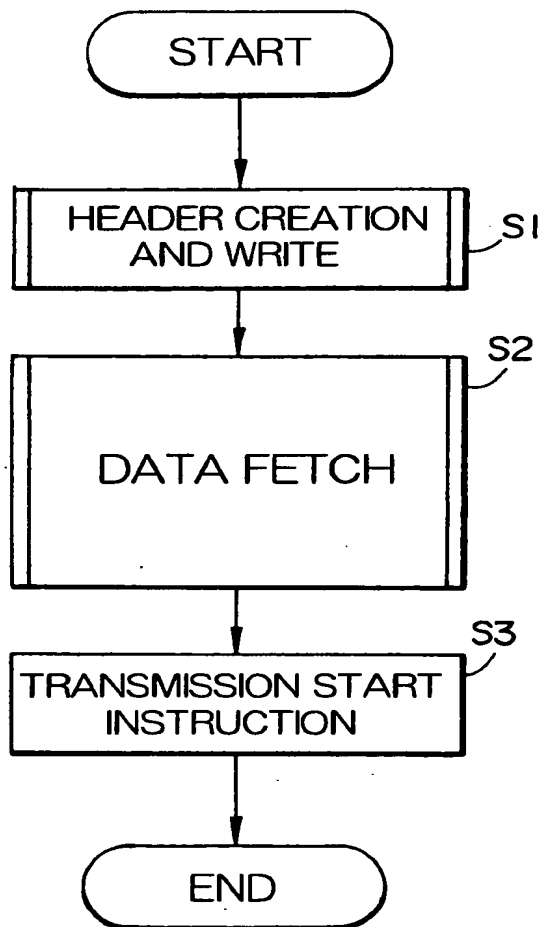
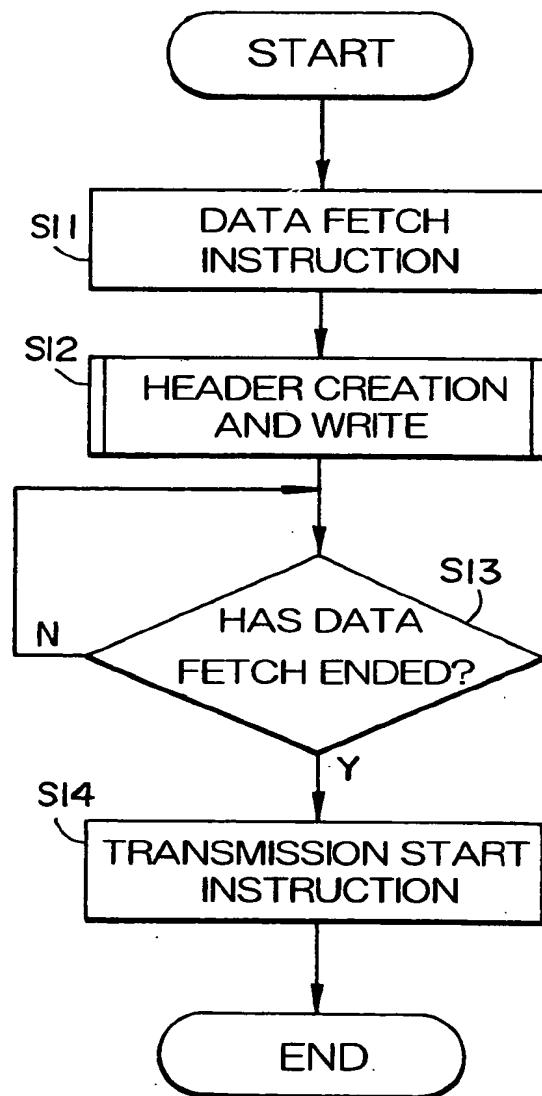
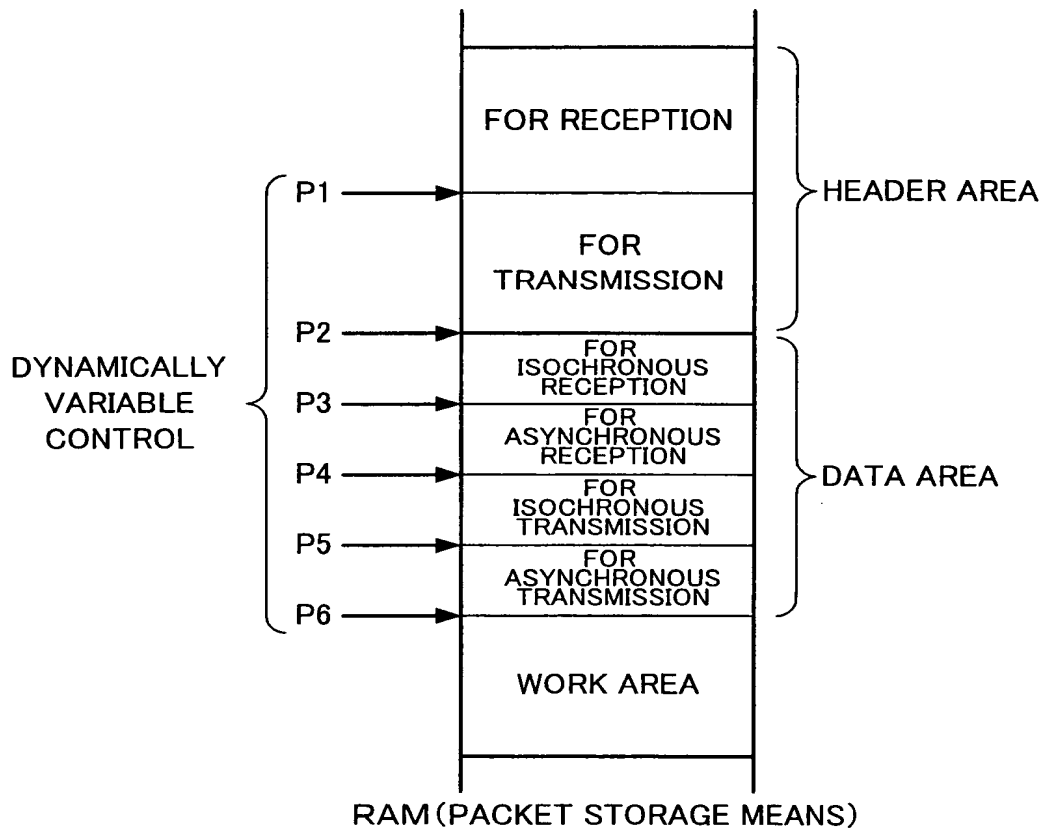


FIG. 16B





**FIG. 17**

**FIG. 18B**

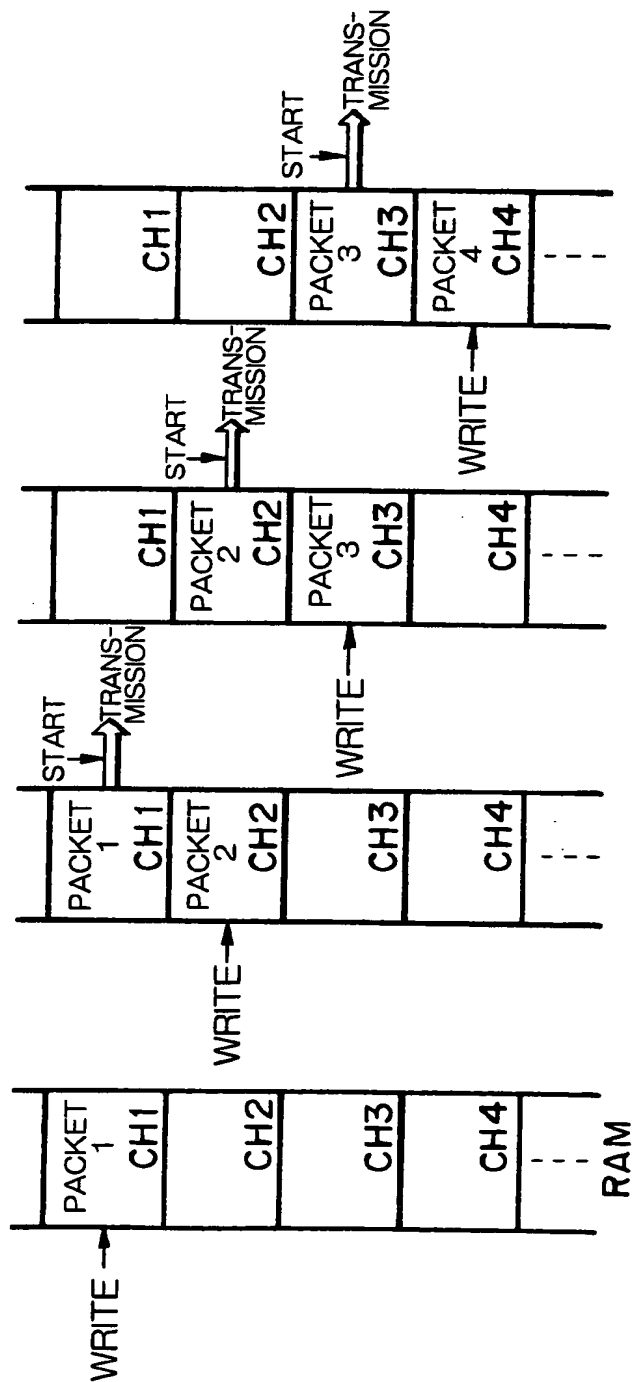
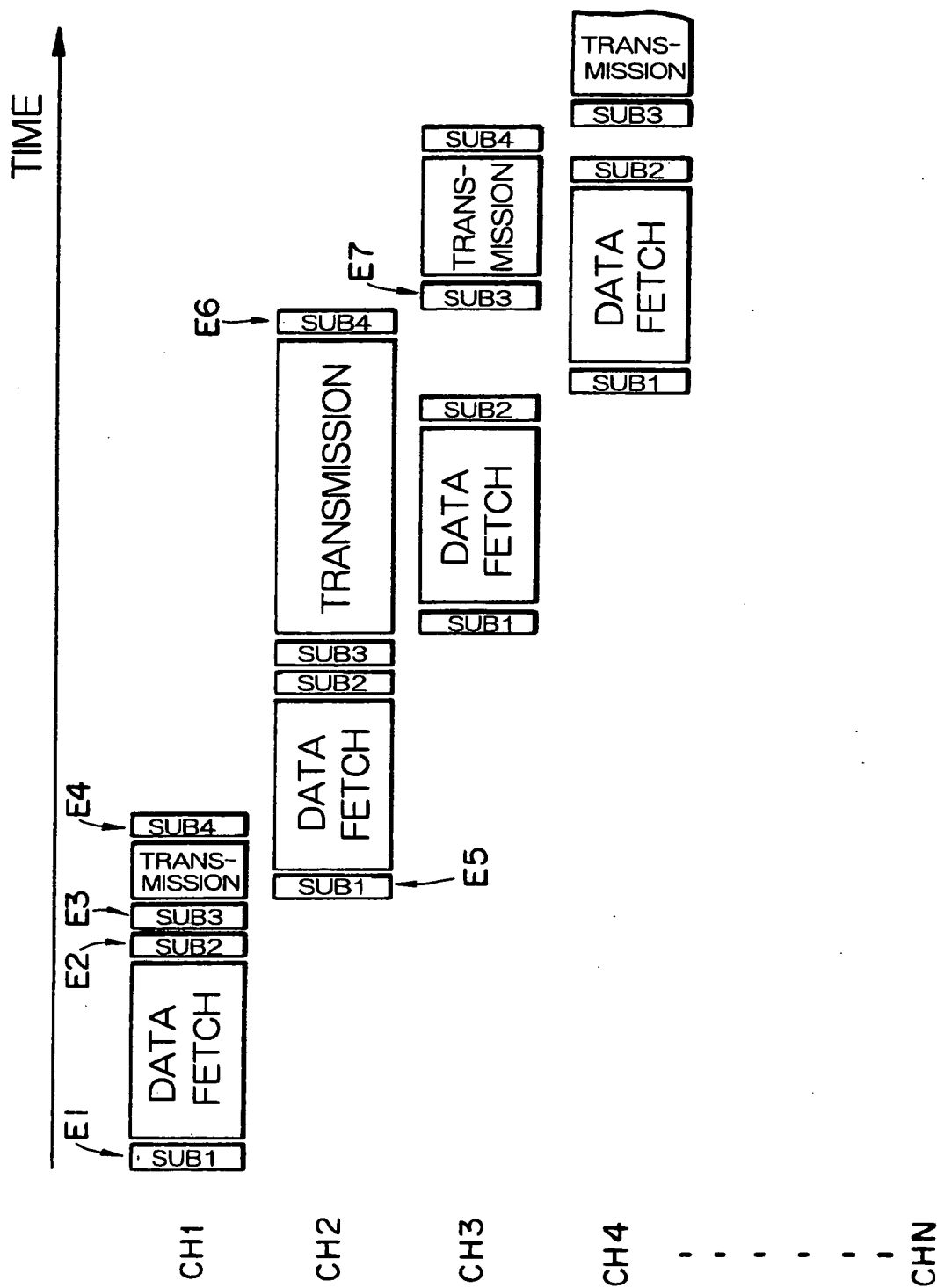
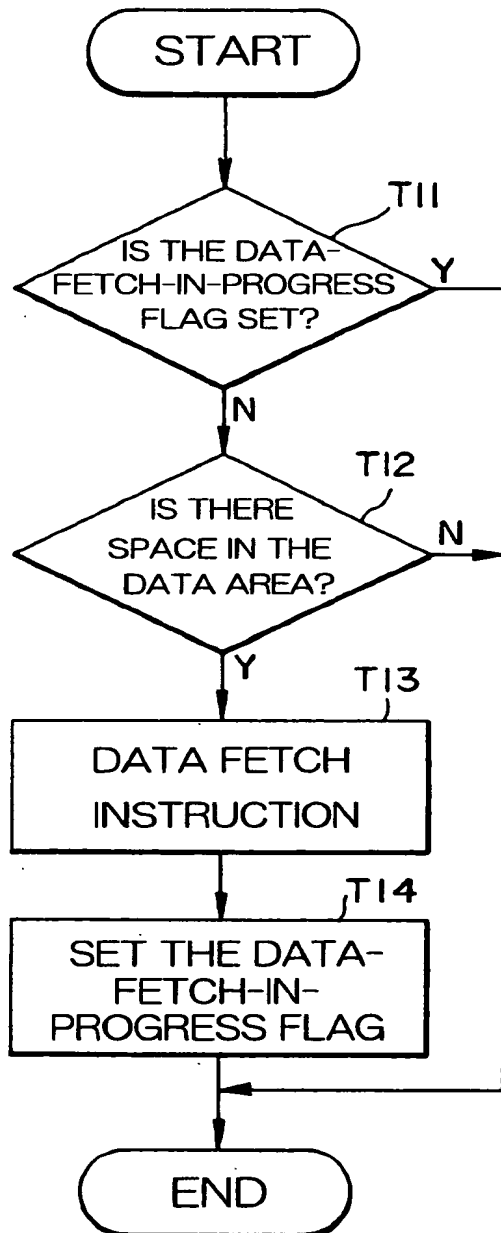
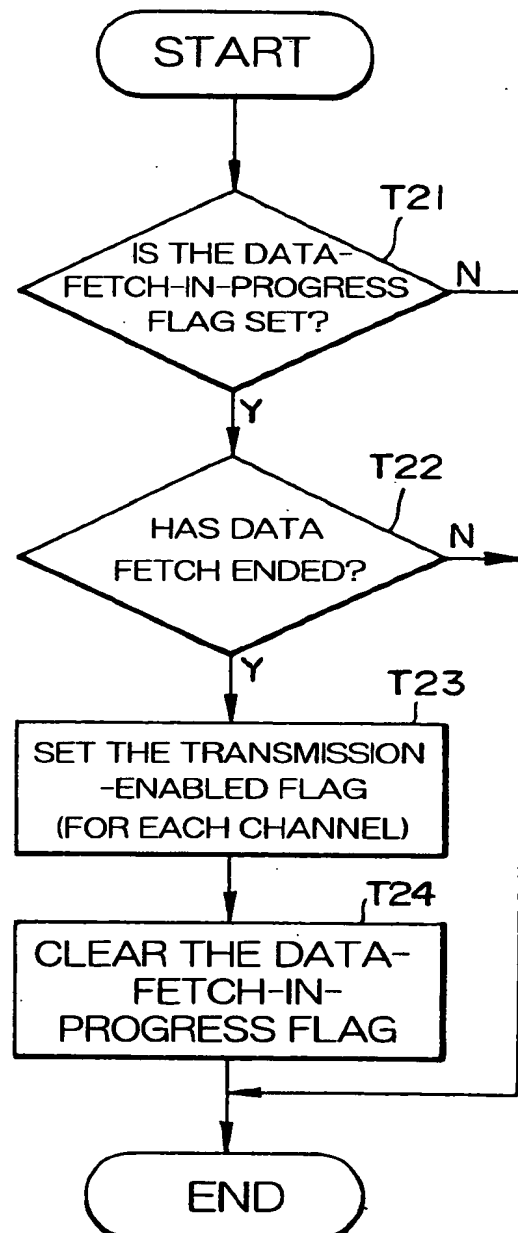


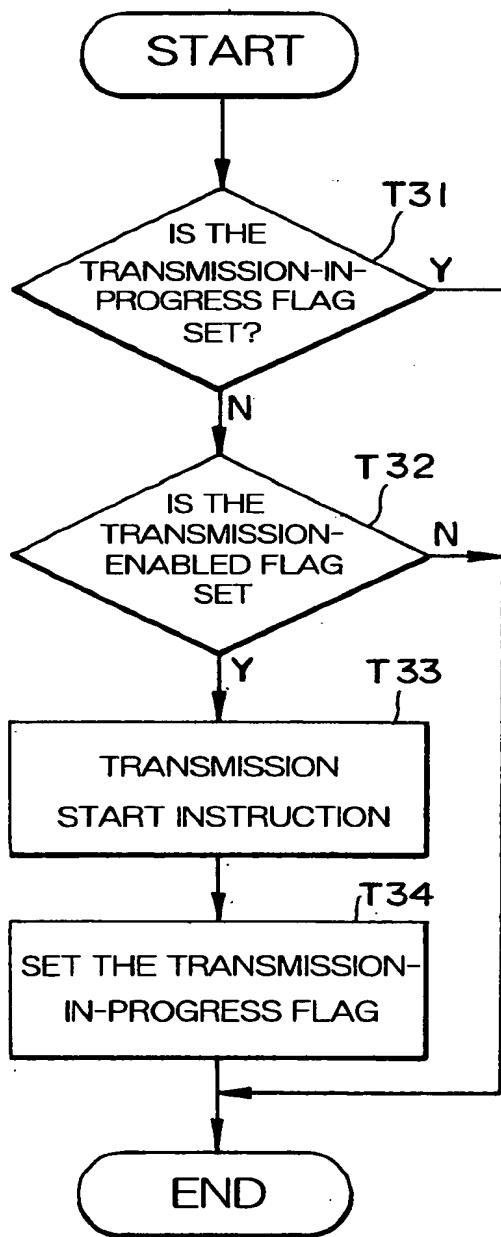
FIG. 19



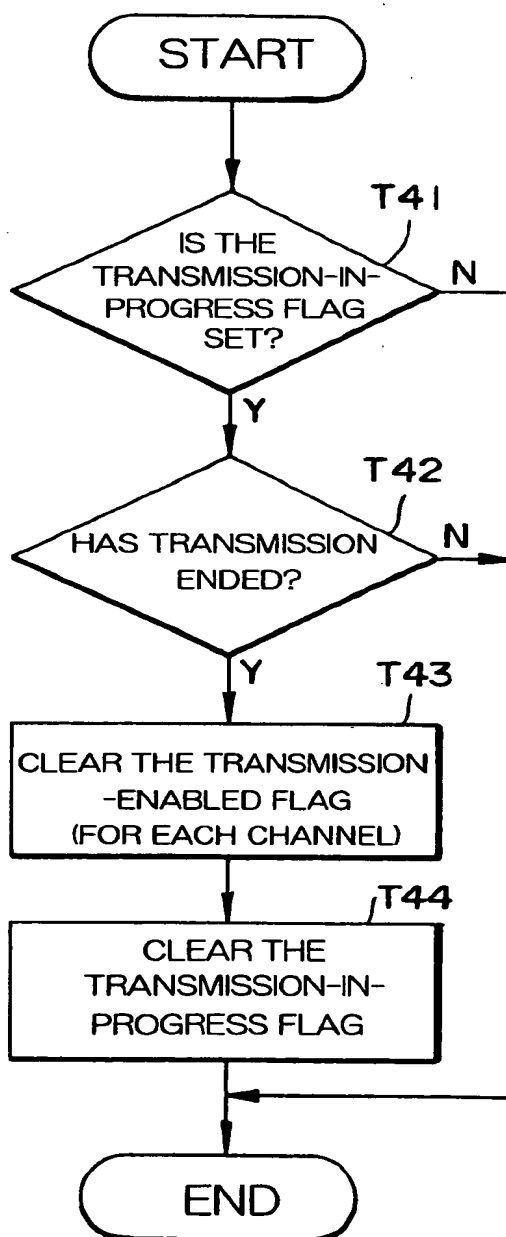
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FIG. 20A  
SUB 1FIG. 20B  
SUB 2

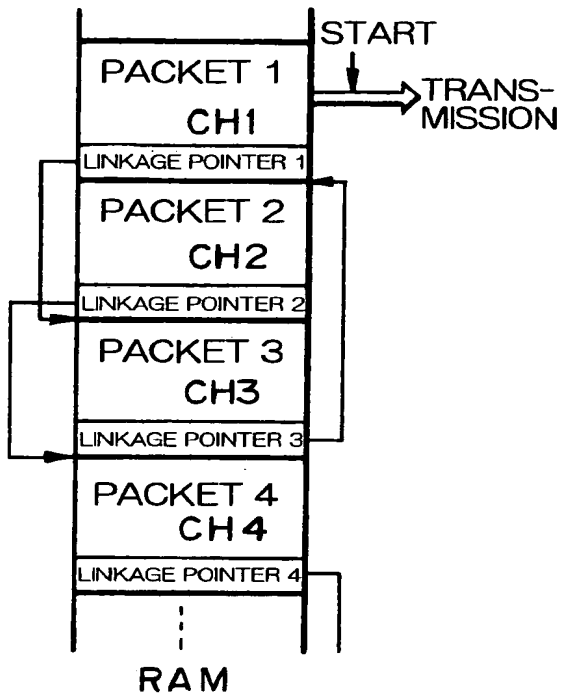
SUB 3



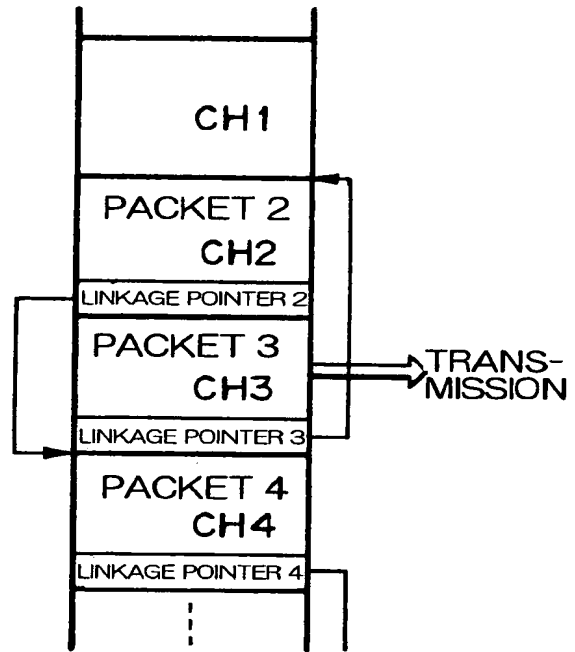
SUB 4



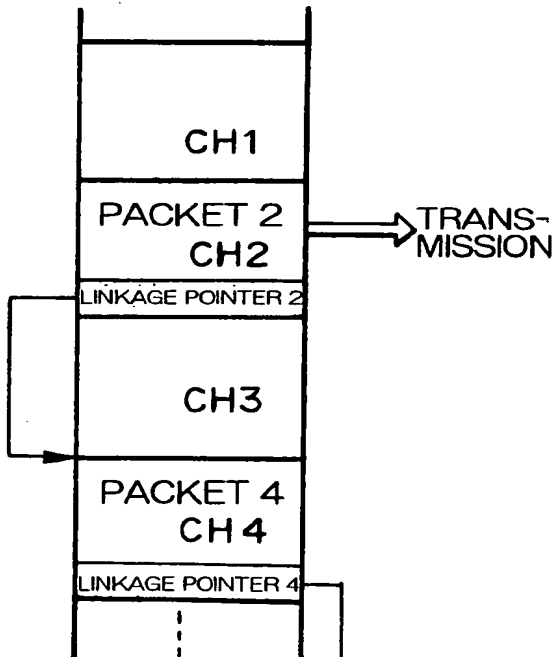
**FIG. 22A**



**FIG. 22B**



**FIG. 22C**



**FIG. 22D**

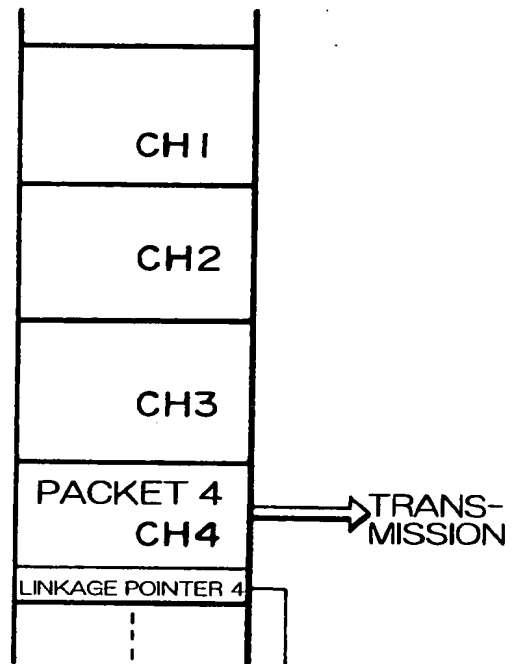


FIG. 23A

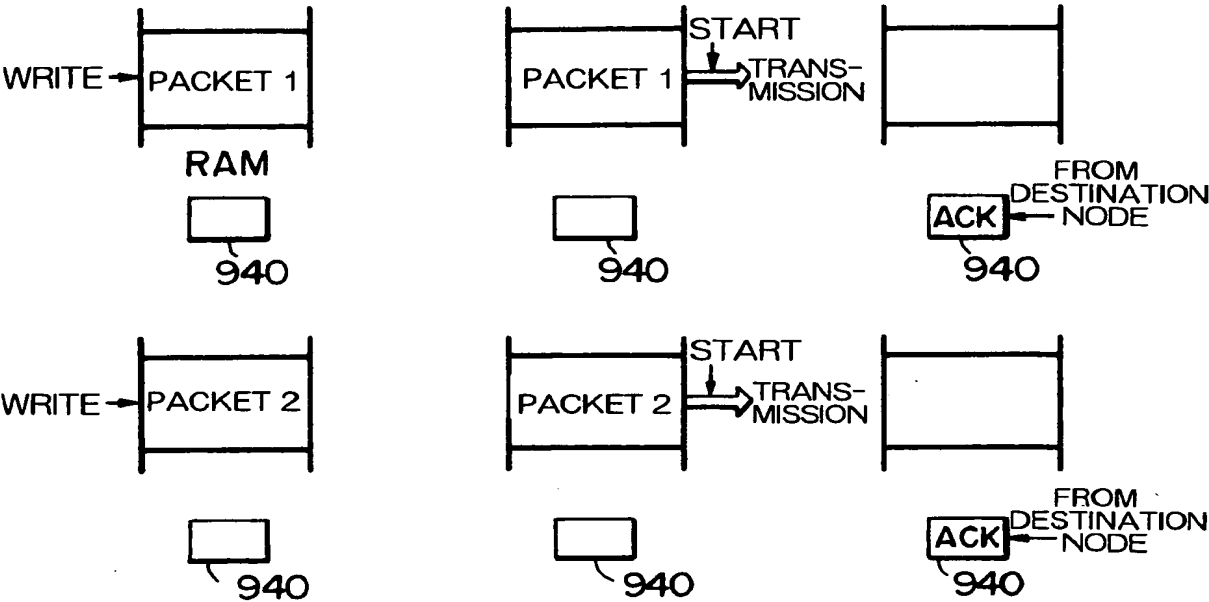


FIG. 23B

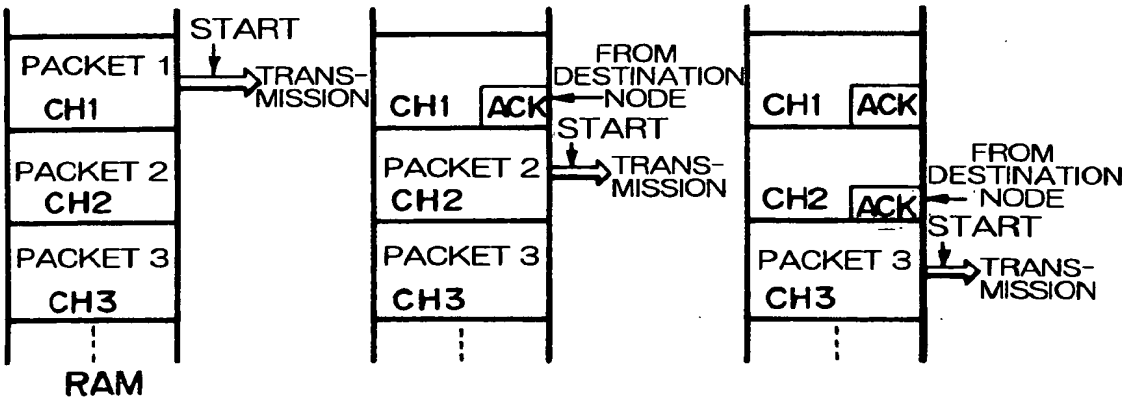


FIG. 23C

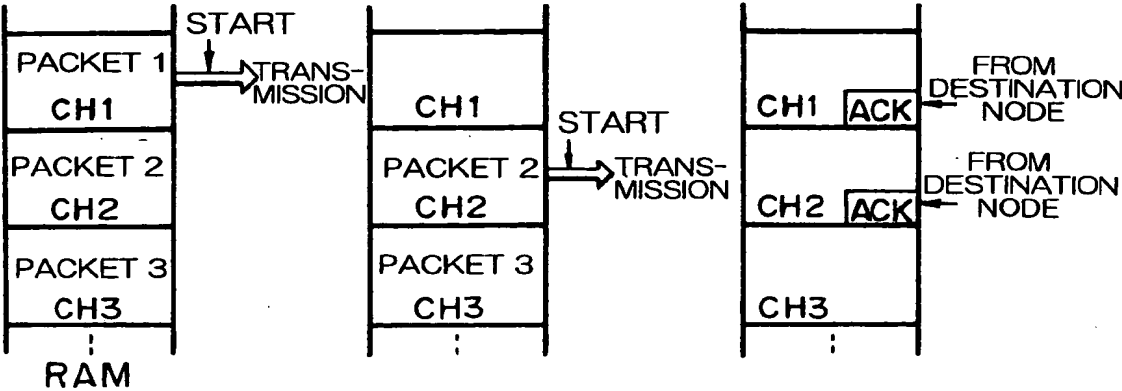


FIG. 24A

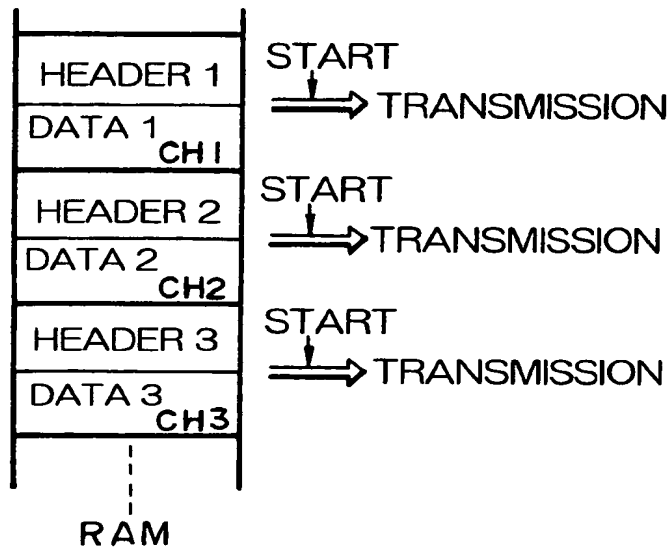
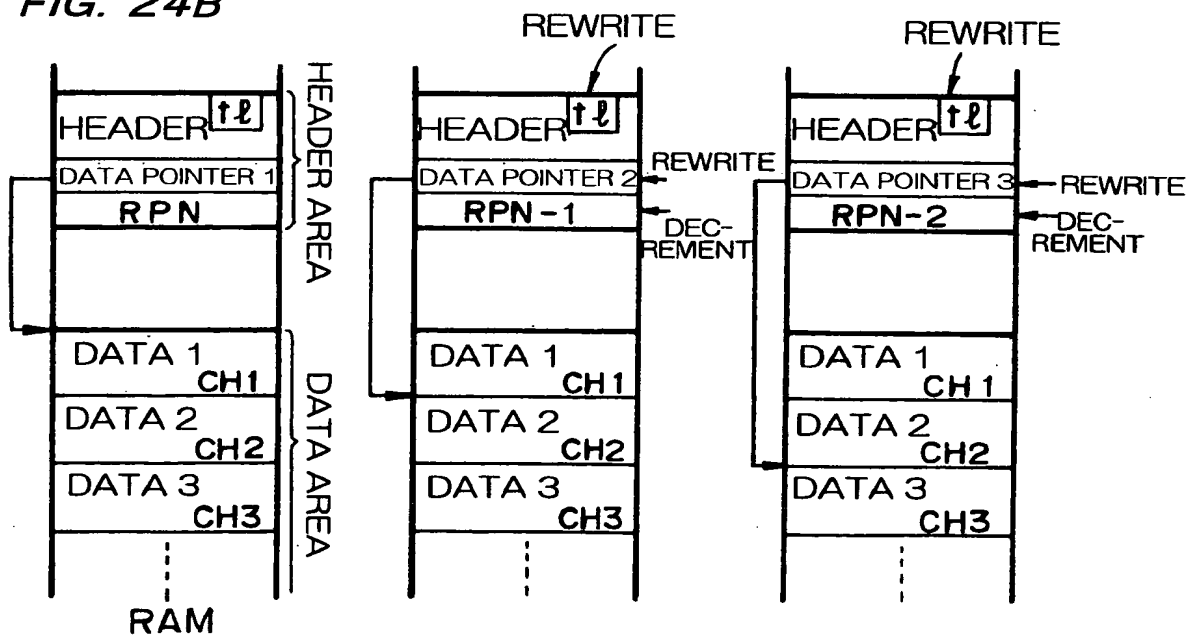


FIG. 24B





The diagram illustrates the timing of data transmission for two channels, CH1 and CH2, over a common time axis. The time axis is represented by a horizontal arrow pointing to the right, labeled 'TIME'.

**Channel CH1:**

- DATA FETCH:** A solid rectangular block.
- TRANSMISSION:** A solid rectangular block.
- Header Creation and Write:** A dashed rectangular block.

**Channel CH2:**

- DATA FETCH:** A solid rectangular block.
- TRANSMISSION:** A solid rectangular block.
- Header Creation and Write:** A dashed rectangular block.

**TRANSMISSION START TIMING:**

- CH1 TRANSMISSION START:** A dashed rectangular block.
- CH2 TRANSMISSION START:** A dashed rectangular block.

The diagram shows that CH1 starts its data fetch and transmission earlier than CH2. The header creation and write phase for CH1 occurs during its transmission phase. The transmission start timing for CH1 is indicated by an arrow pointing to the start of its transmission phase. Similarly, the transmission start timing for CH2 is indicated by an arrow pointing to the start of its transmission phase.

TRANSMISSION  
START TIMING

FIG.25B

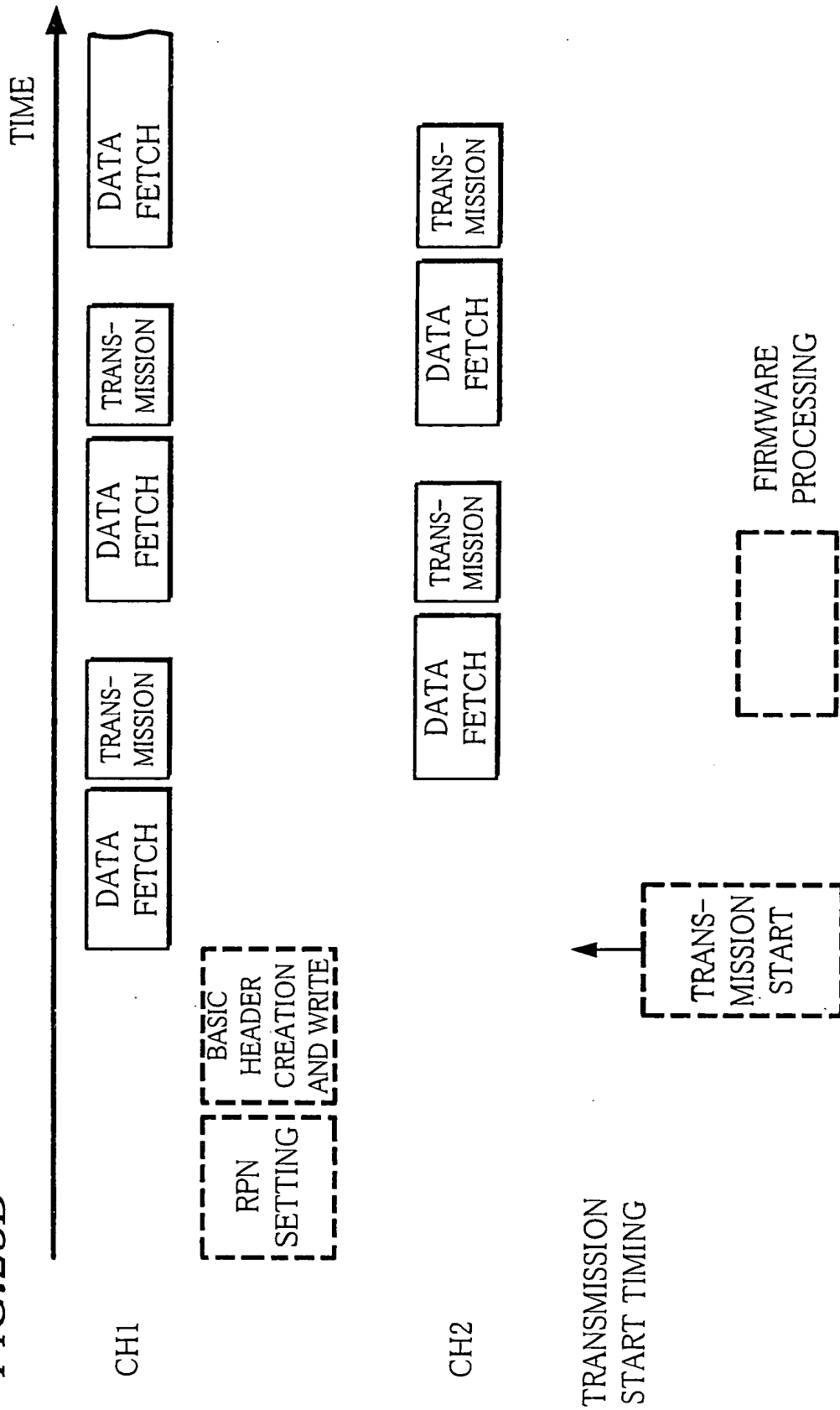
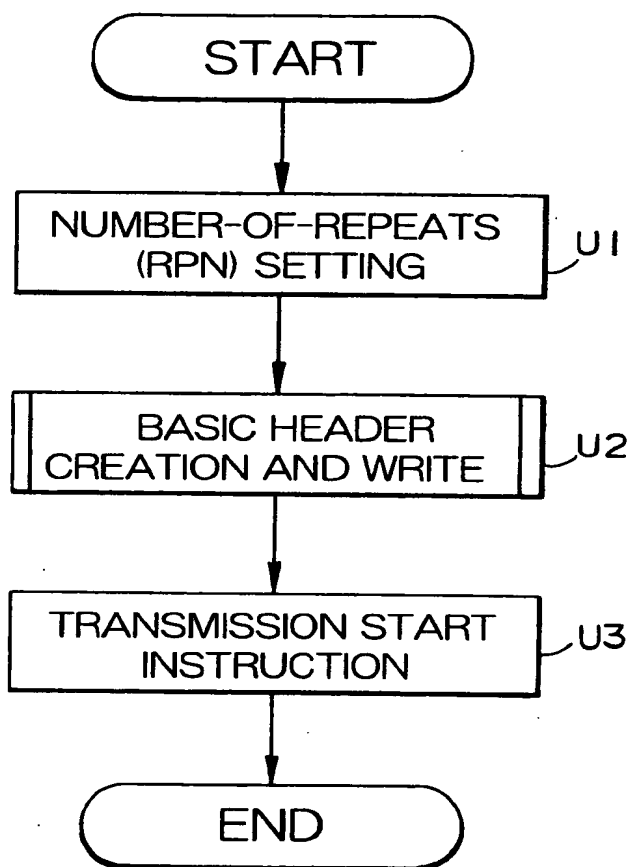


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FIG. 27

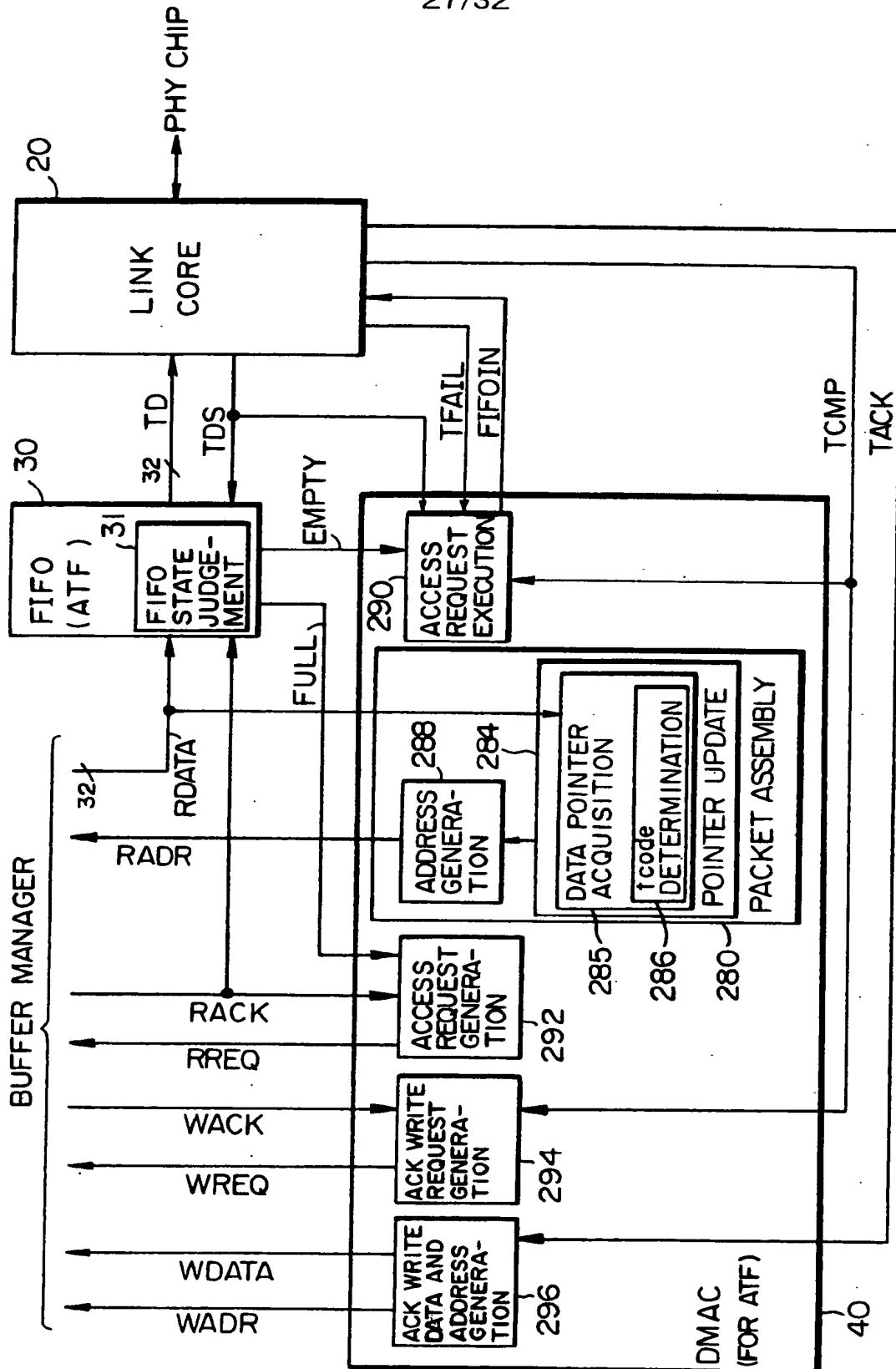


FIG. 28

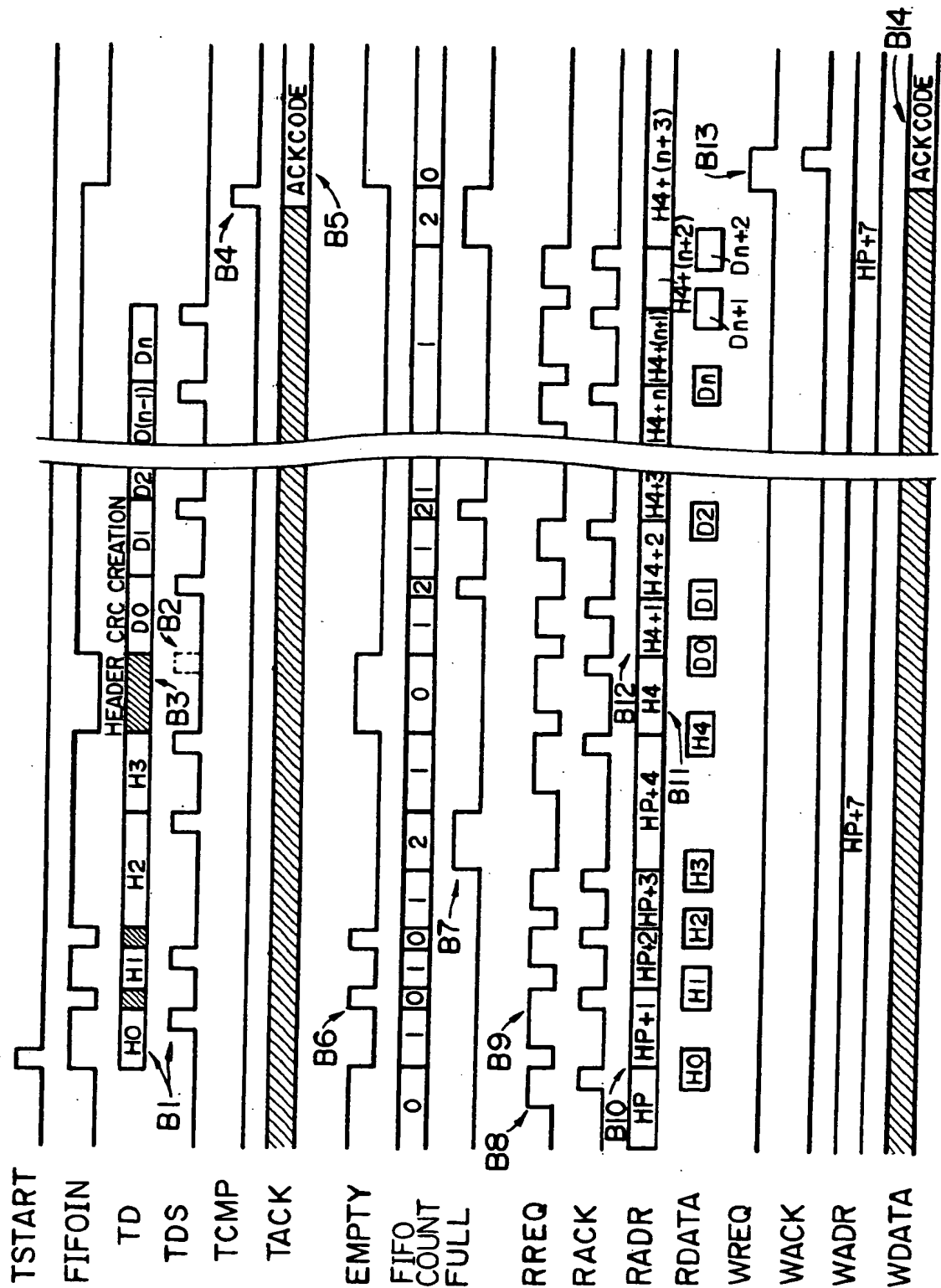


FIG. 29A

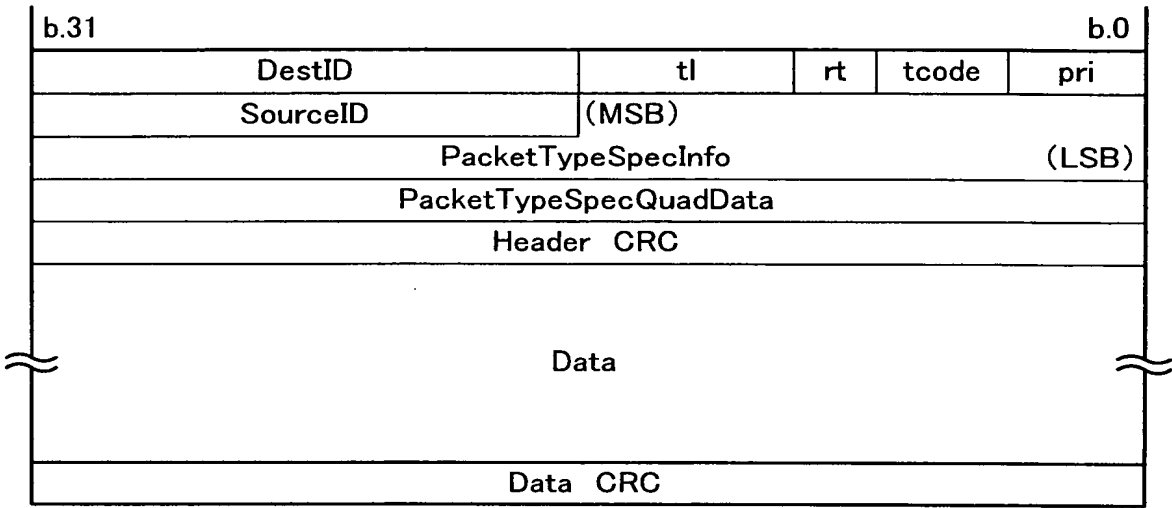


FIG. 29B

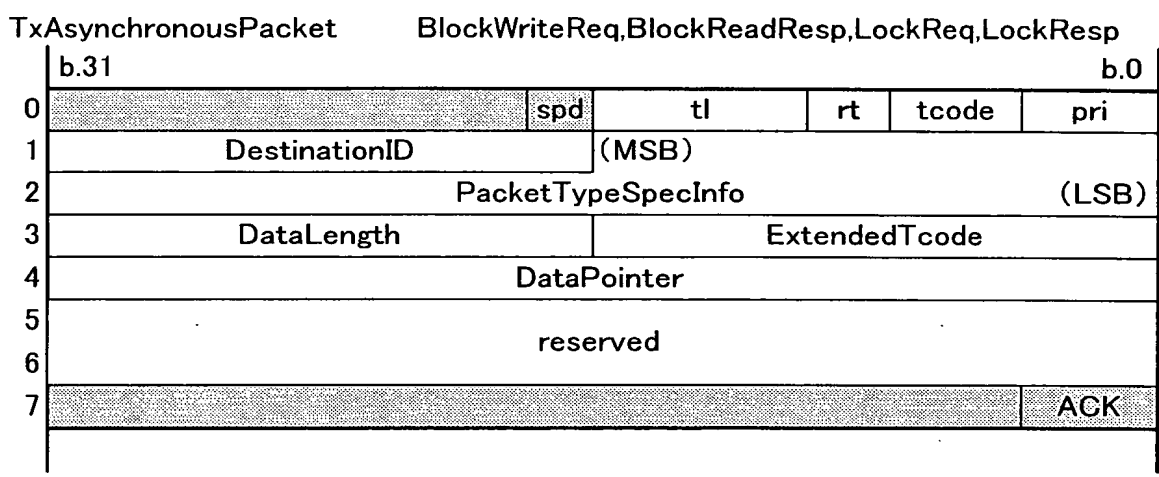


FIG. 30A

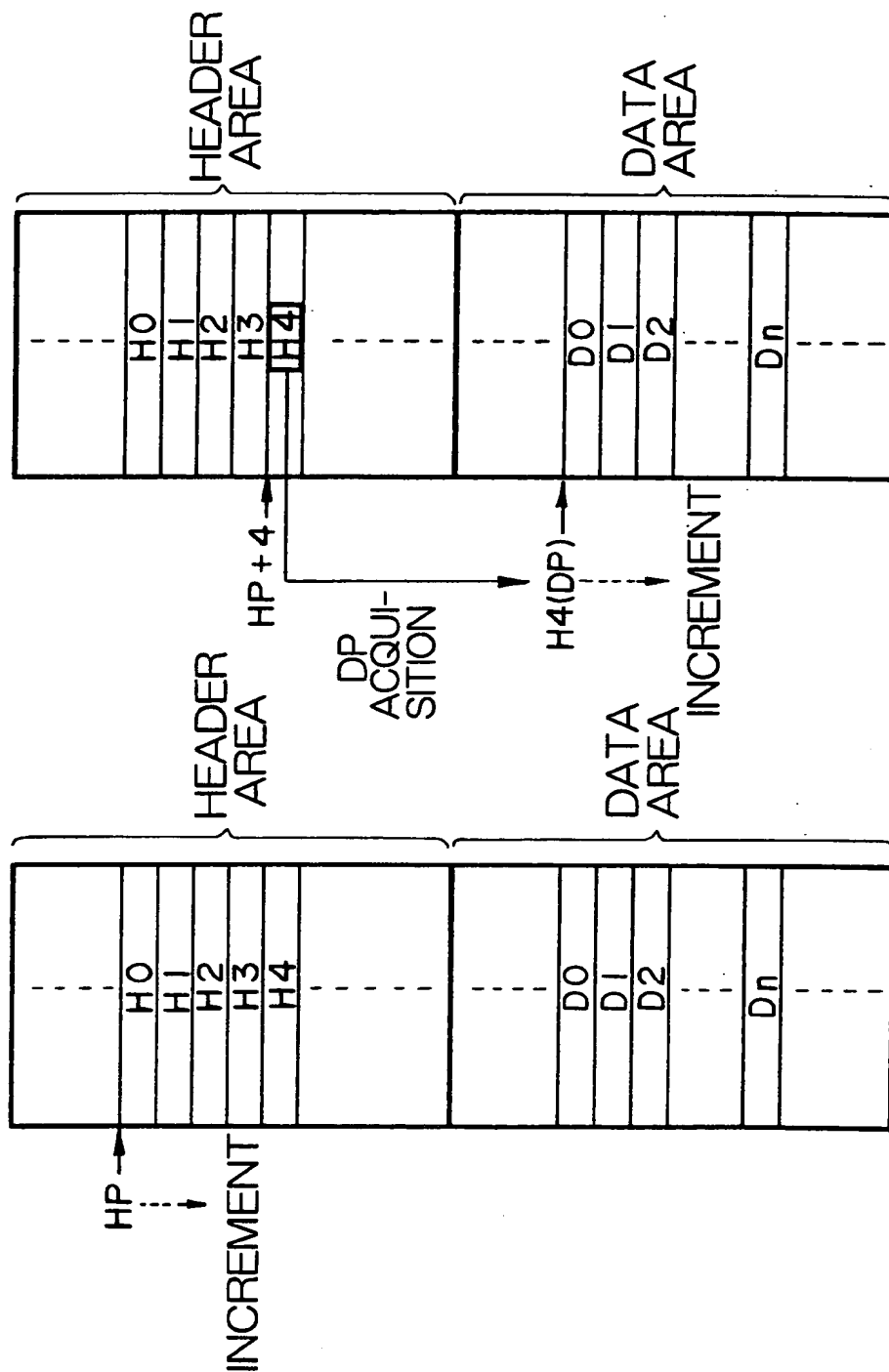
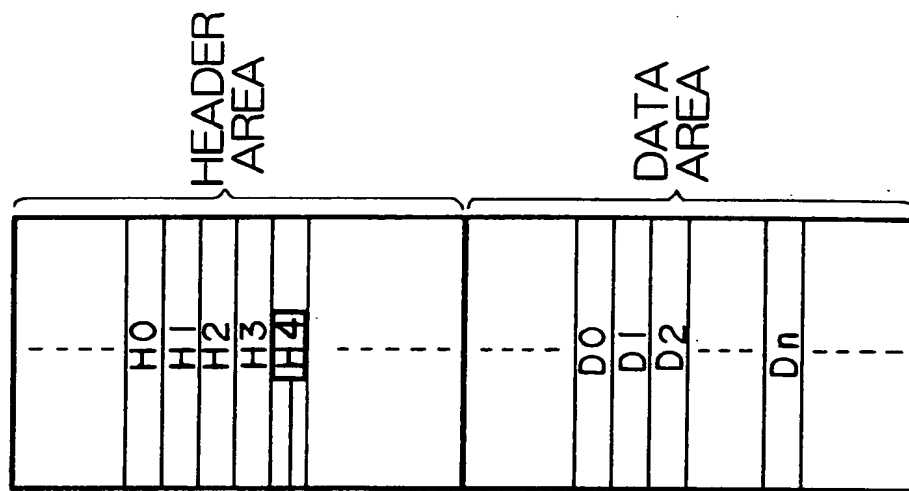


FIG. 30B



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FIG. 31A

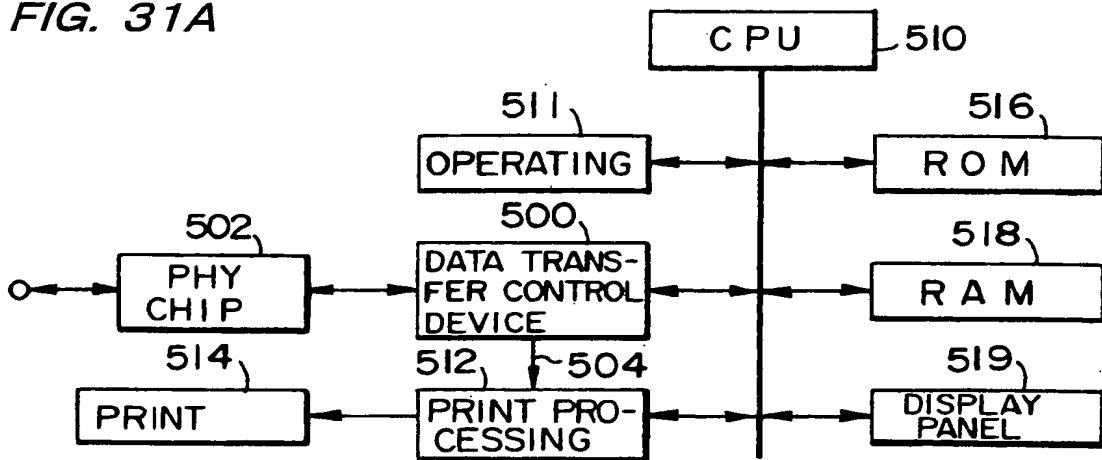


FIG. 31B

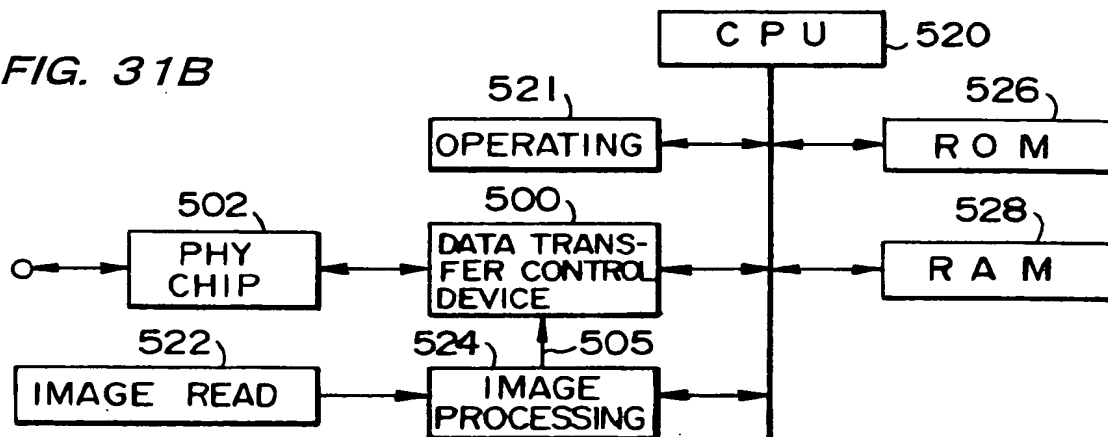
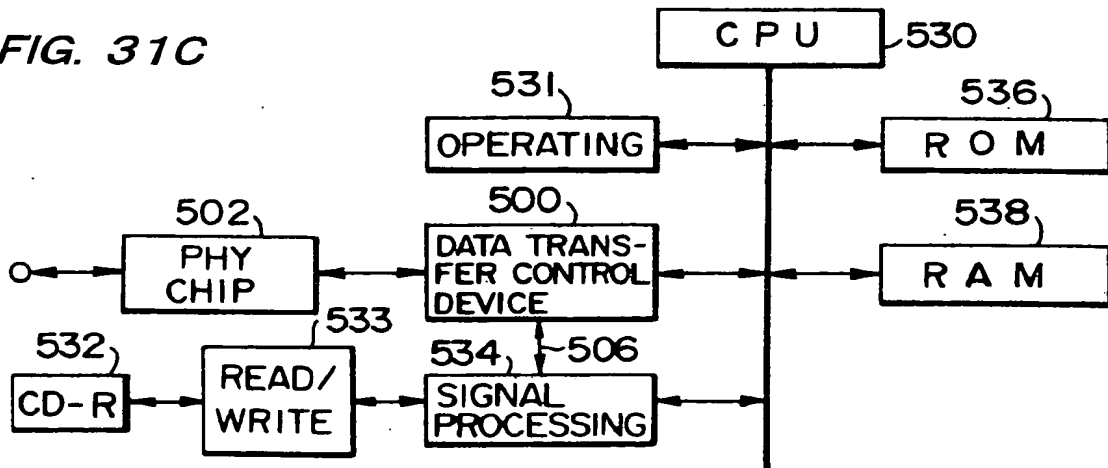
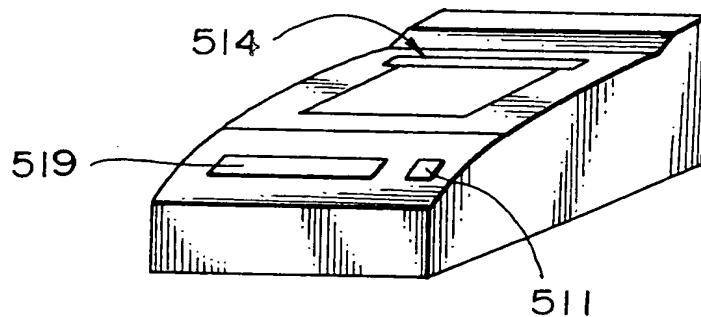


FIG. 31C

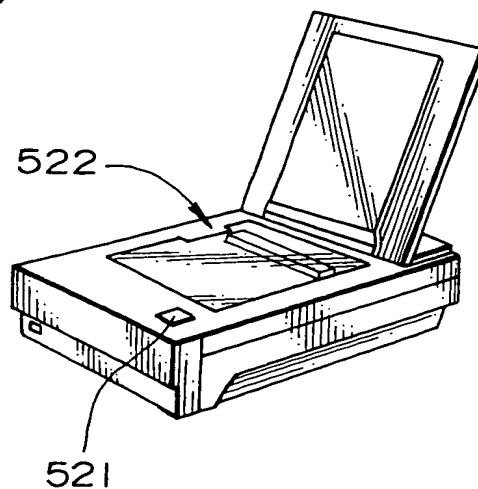




**FIG. 32A**



**FIG. 32B**



**FIG. 32C**

